Self-healing Self-adaptive Low power High Resolution ADC for Space Applications"

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Work accomplished in FY08

Design of a high resolution Cryogenic ADC:

- ❑ System design of a high resolution continuous-time and a discrete-time cryogenic Sigma delta ADC (completed)
- ❑ Study the effect of radiation including SEE and TID (completed)
- ❑ Design of wide-temperature biasing scheme (completed)
- ❑ Design and tape-out of the major building blocks (including low noise switched-capacitor integrators and RC-tunable continuous-time integrators) (completed)
- ❑ Implementing several analog techniques to reduce noise without compromising power and area such as CLS, CHS, fine and coarse sampling,…… (completed)
- ❑ *Tape-out and Test of the whole sigma delta ADC (on going)*

Design Specifications

- ❑ Temperature range: -230 / C to +120 / C
- ❑ 24 Bits at 100 Hz, 20 Bits at 1 KHz
- ❑ Application: Spectroscopy
- ❑ Power efficiency better than 8 pJ/conversion
- ❑ Design technology IBM 0.13 µm

Proposed approach:

Design a tunable sigma delta ADC, use wide-temperature biasing scheme, use different techniques to reduce noise and increased resolution

Design Challenges

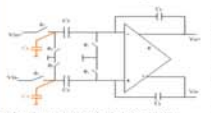
- ❑ the required high resolution limits the switching noise and Opamp noise to a very small value
- ❑ extremely small switching noise requires large capacitors, which results in large area, high power consumption, large capacitive load on Opamps,…. (e.g. 22 Bits at full-scale of 1 V requires sampling capacitors to be larger than 3uF!!)
- ❑ Reducing noise at Opamp requires using larger devices and increased g_m which trades off with power and area.

Proposed Solutions: Problem of Switching Noise (1)

Larger capacitor are required for high resolution ADC

1) Source needs to drive large load
2) Feedback capacitor would be even larger
3) Opamp will see a large capacitive load

Excessive power consumption and silicon area



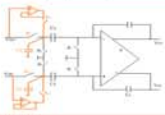
Solution:
Add one set of large capacitor Cx *(could be even off-chip) Cx is large to reduce KT/C noise.
✓ Size Cx based on noise requirement
✓ Size Cs based on matching requirement
✓ Size Cf based on the required gain in the stage

*H. Zare-Hoseini, M.Y. Azizi, O. Shoaei SCS03

Proposed Solutions: Problem of Switching Noise (2)

Adding Cx reduces the loading on the Opamp and the total size of the capacitor but still the source needs to drive large capacitance (now Cx+Cs instead of Cs)

Our proposed solution:
Use a course/fine sampling technique in addition to Cx



It requires an extra clock phase.
Added buffers can be made very low power since their linearity and noise are not important.

Proposed Solutions: Reducing Opamp Noise (1)

Correlated Double Sampling (CDS):
Noise and offset are sampled twice in both clock phases and their final effect gets cancelled.

Reduces flicker noise and offset. The effect of Opamp finite gain is reduced partially. Drawback: increases in-band noise due to noise aliasing.

Chopper Stabilization (CHS):
Modulates the low frequency noise and transfers it to high frequency where it can be filtered out by a low-pass-filter.

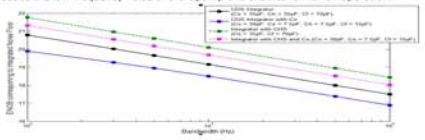
Reduces flicker noise and offset. Does not have the problem of noise aliasing but has no effect on the error caused by Opamp finite gain.

Correlated Level Shifting (CLS*):
Samples the error signal caused by finite gain of Opamp and subtracts it from the output of the Opamp
Best technique to reduce the effect of finite gain of Opamp, provides rail-to-rail operation, has a better noise performance than CDS.

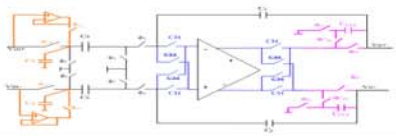
* B. Robert Gregoire, Un-Ku Moon, JSSCC08

Proposed Solutions: Reducing Opamp Noise (2)

- ❑ results show that chopper-stabilization has a better noise performance than correlated-double-sampling (correlated-double-sampling suffers from aliased noise).
- ❑ This design uses chopper-stabilization in addition to correlated-level-shifting to reduce the low frequency noise of the Opamp and enables rail-to-rail operation.

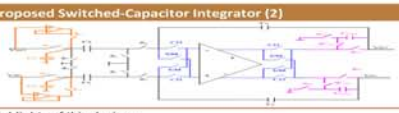


The Proposed Switched-Capacitor Integrator (1)



Φ_{11} input signal is sampled on Cx and Cs through input buffer
Φ_{12} input signal is sampled on Cx and Cs directly
Φ_{21} output signal is sampled on C_{CLS}
Φ_{22} the error due to Opamp finite gain is cancelled from output
CH and $\overline{CH}$ are the two complementary phases used for chopping and they are intentionally chosen not to be relevant to clock period to avoid the cross products between the two clocks.

The Proposed Switched-Capacitor Integrator (2)



Highlights of this design:

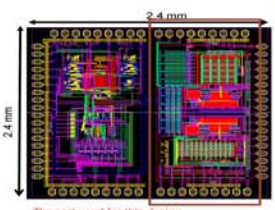
✓ **Uses Cx to reduce the total capacitance required (Cs and Cf), could be even off-chip**
✓ **Uses low-power buffers to relax the driving requirement of the source**
✓ **Uses chopper-stabilization to reduce the flicker noise and offset of the Opamp**
✓ **Uses CLS that enables rail-to-rail operation (maximizes signal power) as well as low gain Opamp**

Result: Low power, high resolution design using low gain fast Opamps and small caps

Tape-out of Building Blocks

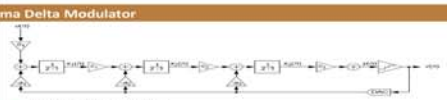
A tape-out in March had all major building blocks of a high-resolution DT sigma-delta modulator:
Chopper stabilization and correlated doubles sampling techniques for switched-capacitor gain amplifiers and integrators.

JAZZ 0.18um Technology



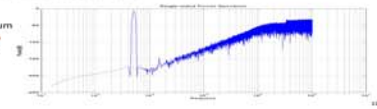
The part used for this design

Sigma Delta Modulator

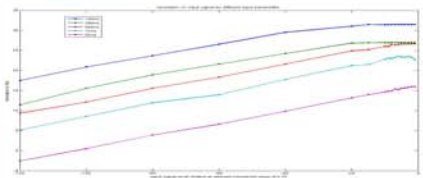


- Standard CIFF structure
- 3rd order, can be reconfigured as a 2nd order
- Optimized and tunable coefficients

Output spectrum



Scaling Resolution with Speed



Speed-resolution is scalable in Sigma Delta Modulators

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